Microfabrication of microsystem-enabled photovoltaic (MEPV) cells

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ABSTRACT

Microsystem-Enabled Photovoltaic (MEPV) cells allow solar PV systems to take advantage of scaling benefits that occur as solar cells are reduced in size. We have developed MEPV cells that are 5 to 20 microns thick and down to 250 microns across. We have developed and demonstrated crystalline silicon (c-Si) cells with solar conversion efficiencies of 14.9%, and gallium arsenide (GaAs) cells with a conversion efficiency of 11.36%. In pursuing this work, we have identified over twenty scaling benefits that reduce PV system cost, improve performance, or allow new functionality.

To create these cells, we have combined microfabrication techniques from various microsystem technologies. We have focused our development efforts on creating a process flow that uses standard equipment and standard wafer thicknesses, allows all high-temperature processing to be performed prior to release, and allows the remaining post-release wafer to be reprocessed and reused. The c-Si cell junctions are created using a backside point-contact PV cell process. The GaAs cells have an epitaxially grown junction. Despite the horizontal junction, these cells also are backside contacted. We provide recent developments and details for all steps of the process including junction creation, surface passivation, metallization, and release.

Keywords: Microsystems enabled photovoltaics, micro solar cells, miniature solar cells, fabrication

1. INTRODUCTION

This paper describes the design and fabrication of miniature silicon solar cells that are created using microsystem tools and techniques. These miniature solar cells create a new class of photovoltaics with potentially novel applications and benefits such as dramatic reductions in cost, weight, and material usage.

We discuss the fabrication details of cells fabricated in two different types of crystalline silicon and crystalline GaAs. Each cell type takes advantage of a mechanism for detaching the first 1-20 μm of material from the top of the wafer to create the cells, leaving the rest of the material for future reuse. The crystalline silicon cells are released using either hydrofluoric acid (HF) with silicon-on-insulator (SOI) wafers (referred to as the radial electrode design), or potassium hydroxide (KOH) with (111) oriented wafers (referred to as the linear electrode design). The gallium arsenide cells are released using an aluminum arsenide release layer and a HF release chemistry, similar to epitaxial lift-off (ELO)[1], but without the supporting release handle typically used. Figure 1 provides an image of a representative crystalline silicon cell.

There is an obvious advantage to creating very thin solar cells, particularly with high-cost crystalline semiconductor materials. By reducing the thickness to the minimum required to obtain adequate absorption, significant materials savings can be realized. Figure 2 illustrates the cost savings realized by reducing the thickness of the silicon cells.

In addition, by reducing the lateral dimension of the solar cells, other scaling benefits are realized[2,3,4,5,6]. These benefits improve PV cell, module, and system performance; lead to new functionality not available with traditional cell technologies; and ultimately lead to multiple pathways to reduce cell, module, and system costs.

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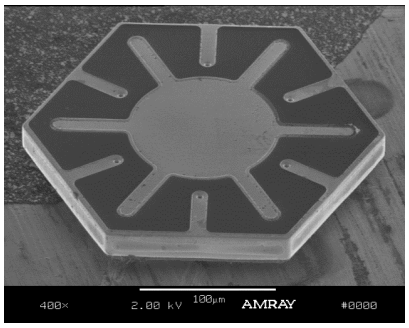


Figure 1. SEM image of a 20 micron thick, 250 micron across crystalline silicon cell.

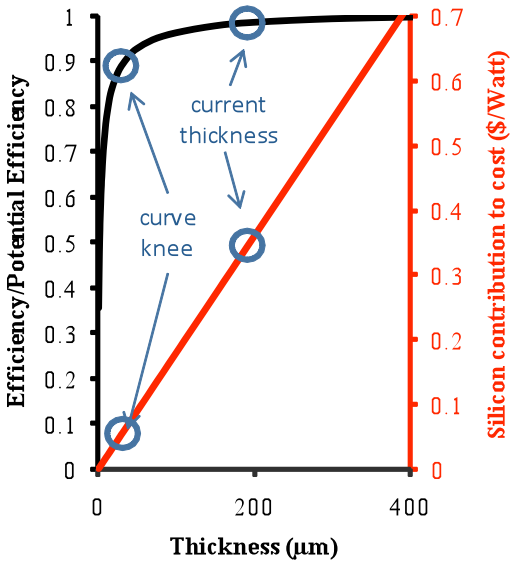


Figure 2. Cost and potential conversion efficiency as a function of silicon solar cell thickness.

2. SILICON ON INSULATOR (SOI) CRYSTALLINE SILICON CELLS

2.1 Design

Figure 3 illustrates the various designs for the SOI-based cells, referred to as the radial designs. The n-implantation is in the center and the p-implantation is on the outer rim. Fingers of n-implanted dopants go from the center contact towards the edge without touching the edge, and p-implanted fingers go from the edge towards the center without touching the center. The purpose of these fingers is to reduce the space between the p and n-areas and thus enhance carrier collection. The metal contact layer follows the same shape as the implantations below, but only contacts the semiconductor in very small areas (point contacts) through a nitride layer.

The design for the radial cell consists of five photolithographic masks. The first mask defines the p-implantation areas. The second defines the n-implantation areas. The third mask defines the small windows that allow the metal to contact the implanted silicon areas through the silicon nitride passivation layer. The fourth mask defines the radial interdigitated metal contact pattern. The fifth mask defines the lateral size and the hexagonal morphology of the cell.

2.2 Fabrication

The fabrication process is illustrated in Figure 4 and begins with a 6 inch, SOI wafer, 20-30 Ω-cm, p-type, (100) oriented wafer to create the junctions. The device layer is 20 µm thick and the buried oxide layer (BOX) was 1 µm thick.

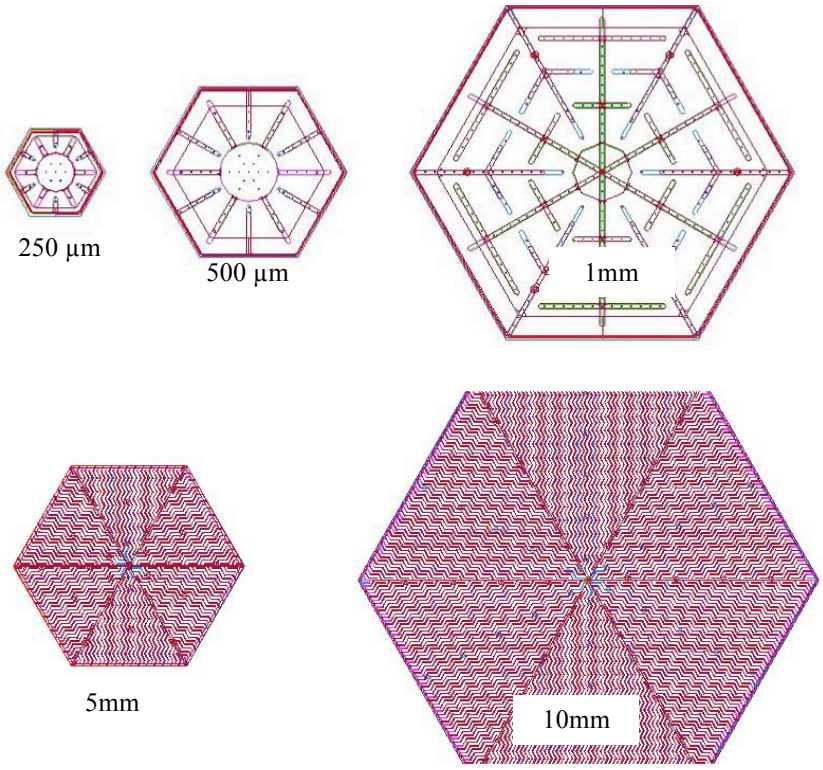


Figure 3. CAD drawings of masks designs for the radial solar cells of various lateral sizes.

The first process steps are the p and n-type dopant implants. Implantations of boron (energy = 45 keV) and phosphorus (energy = 120 keV) are made with a dose of 3×10^{15} cm^{-2}, tilt of 7°, and range of 0.15 µm for both dopants. A photolithography patterned 1.8 µm thick photoresist layer on top of 300 nm LPCVD silicon nitride and 500 nm CVD silicon oxide is used to selectively mask the implantations. A drive-in step is performed for 30 minutes at 900° C in a N_2 atmosphere.

The next process step opens windows in a low pressure chemical vapor deposited (LPCVD) silicon nitride film for the electrical point contacts to the silicon below with an RIE etch.

Once the windows are opened, the metallization layer is deposited by sputtering. The metallization is a stack of Ti silicide (Ti is deposited and then annealed to interdiffuse with the silicon), aluminum/silicon, and Ti nitride (52 nm, 720 nm and 50 nm in thickness, respectively). Ti silicide reduces contact resistance and provides a barrier to avoid spiking of aluminum through the doped silicon contact. Aluminum/silicon was the main conductor, and Ti nitride serves as a protection from the subsequent wet HF release etch. The metal stack was patterned and etched to define the radial interdigitated metal contacts.

The next process step is a deep reactive ion etch (DRIE) or "Bosch process" to define the side-walls of the cells. The etch process, optimized for an etch depth of 20 µm, uses sulfur hexafluoride (SF_6) as the etchant, and a 2.2 µm thick patterned photoresist as a mask. The etch is designed to land on the buried oxide layer without substantial overetch to avoid footing effects.

After metallization and the creation of the 20 µm deep trench, the final release etch is performed. For this step, the wafer is submerged in a 49% hydrofluoric acid (HF) solution with Tergitol™ (non-ionic surfactant used to wet silicon surfaces). The solution accesses the buried oxide through the trenches and release holes. Depending on the spacing between the trenches and etch release holes, the release can take from 30 to 90 minutes. The substrate is suspended such that the cells fall away from the substrate due to gravity. Finally, the cells are filtered and rinsed with water until the pH is neutral and then transferred to a vial with IPA.

Figure 5 shows a SEM picture and an optical profilometer image of a released 20 μm thick, 1 mm wide silicon cell. Note that only the device layer (20 μm of material) of the original wafer is consumed in the creation of the cells, leaving the handle wafer available for reprocessing.

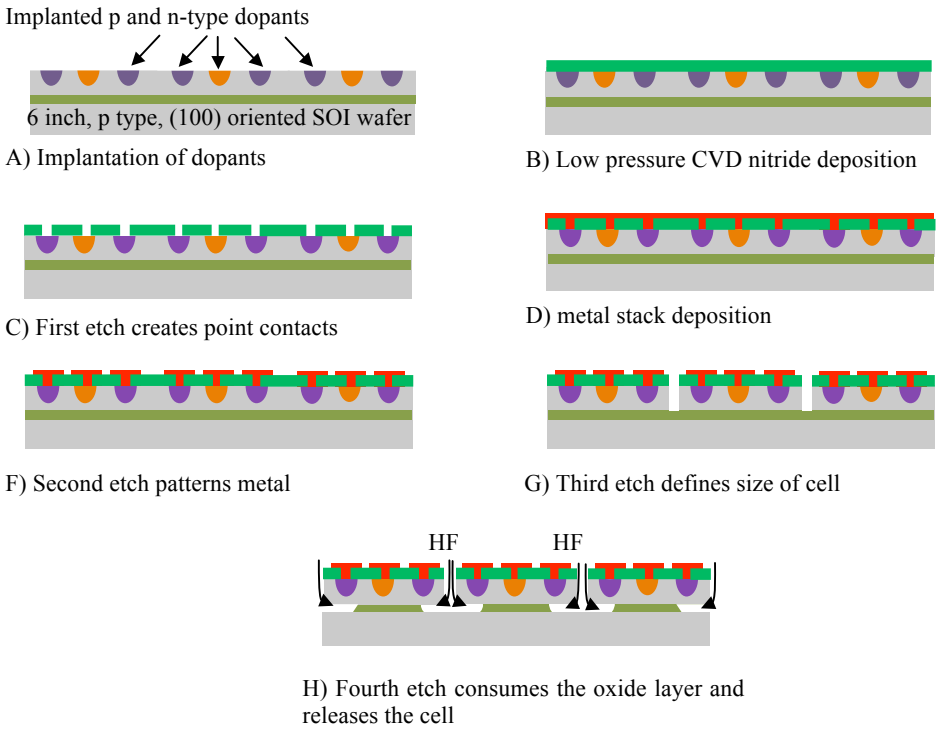


Figure 4. Cross section illustration of the process flow for the creation and release of the cell using a SOI wafer.

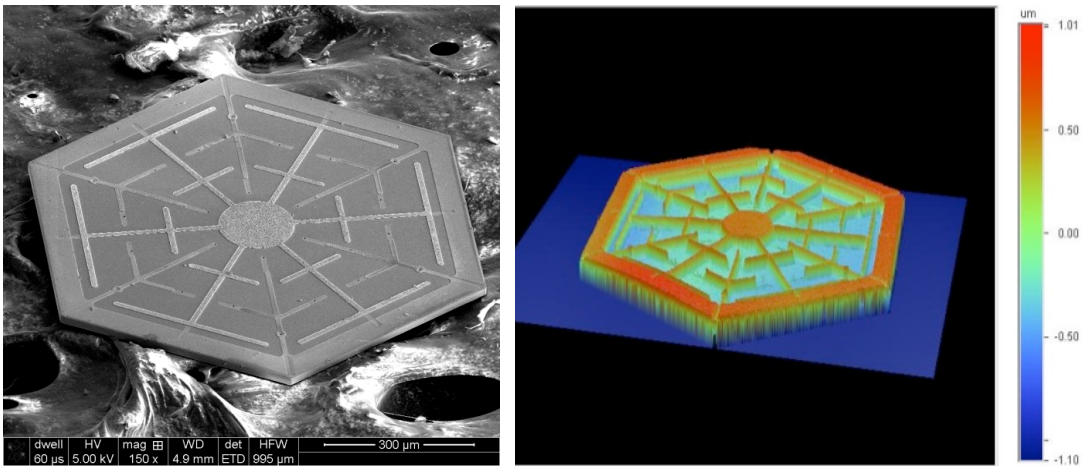


Figure 5. SEM and optical profilometer image of a 1mm solar cell.

3. (111) CRYSTALLINE SILICON CELLS

3.1 Design

The second approach used to fabricate crystalline silicon cells utilizes the crystal plane selective potassium hydroxide (KOH) silicon etchant. Figure 6 illustrates the various designs for these cells, referred to as the linear designs. These designs use linear interdigitated metal contact fingers to bring the collected carriers to contacts on either side of the cell. The n and p-type dopant implantations are performed as spot implants at alternating positions across the backside of the cell. There are two cell sizes with variations on the size and spacing of the implantation locations for both cell sizes, as indicated in Figure 7 and Table 1.

The design requires six photolithographic masks. The first mask defines small circular p-implantation areas. The second defines the n-implantation areas. The third defines the side-walls of the cell. The fourth defines the windows for the point contacts from the metal to the implanted areas through the passivation layer. The fifth mask defines the linear interdigitated metal contact pattern. The sixth mask defines the KOH access trenches for the subsequent release.

3.2 Fabrication

The fabrication process for the linear contact cells, illustrated in Figure 8, begins by implanting alternating p and n-type dopants into regions of the sizes indicated in Table 1 on a 6 inch, 700 μm thick, 3-20 Ω, CZ semiconductor grade, p-type, (111) oriented wafer to create the junctions. Implantations of boron (energy = 45 keV) and phosphorus (energy = 120 keV) are used with a dose of 1×10^{15} cm^{-2}, tilt of 7°, and range of 0.15 μm for both dopants. A photolithography patterned 2.2 μm thick photoresist is used to selectively mask the implantations. A drive-in step is performed for 30 minutes at 900° C in a N_2 atmosphere.

After the junction is completed, a DRIE etch step is performed with a target depth of 20 μm using SF_6 as the etchant and a 2.2 μm thick, photolithography patterned photoresist as a mask. This etch creates trenches that are 2 μm wide which define the sidewalls of the cells. These trenches are filled with a 1 μm thick, conformal silicon nitride layer deposited by LPCVD. The objective of this film is twofold; 1) form the wall that protects the cell from the wet chemistry during the KOH release etch, and 2) passivate the sidewalls of the cell.

The next process step is a reactive ion etch (RIE) of the silicon nitride layer through a 1.8 mm thick patterned photoresist mask. This opens small windows for the metal contacts to be made to the doped silicon regions. After the windows are opened, a 200 nm layer of low-stress tungsten is deposited using plasma enhanced chemical vapor deposition (PECVD). The tungsten is subsequently patterned and RIE etched to define the interdigitated metallization structure on the cell.

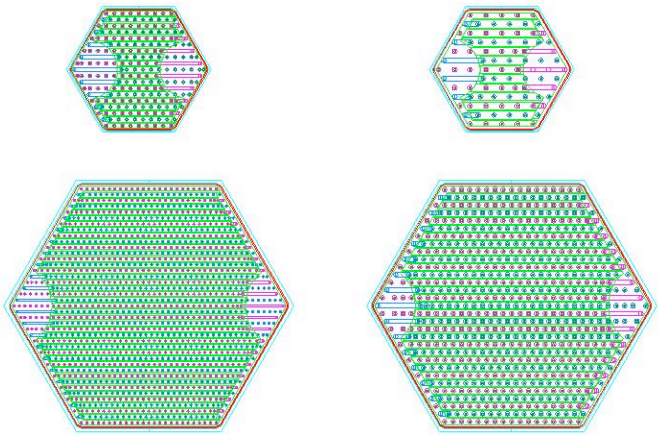


Figure 6. 250 micron and 500 micron linear contact cell designs with interdigitated fingers.

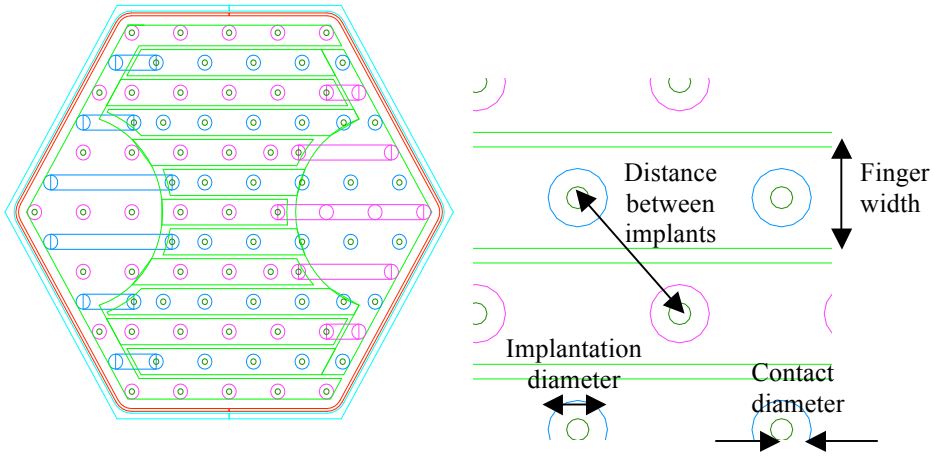


Figure 7. Left: AutoCAD design of a 250 µm wide solar cell (back side contacted) with interdigitated fingers. Right: detail of the implantations and fingers.

Table 1. linear contact cell dimensions.

Size of cell and design	**Distance between implantations (µm)**	**Width of finger (µm)**	**Diameter of implantation (µm)**	**Diameter of contact (µm)**
250 µm tight	13	8.9	6	3
250 µm relaxed	21	13.9	8	3
500 µm tight	12.2	8.6	4	2
500 µm relaxed	15.3	11.5	8	3

The next step of the process is a second DRIE etch with a targeted depth of 25 µm. This etch uses a 1.8 mm thick layer of photoresist, and creates a trench around the periphery of each cell to allow the release etchant access to the sacrificial silicon.

The release of the silicon cells is accomplished by submerging the wafer in a potassium hydroxide (KOH) 6M solution held at 85°C for 3 hours and 45 minutes and then left 24 hours at room temperature to detach the cells from the wafers. The solution accesses the unprotected silicon through the channels formed during the third etch. Due to the orientation dependent etch rates, the (111) planes (parallel to the surface of the wafer) are etched very slowly. The silicon nitride walls defined earlier protects the silicon enclosed by them that would otherwise be etched away. The average etch rate selectivity observed between the (111) and other crystal planes was 1:19, making the fabricated cells thinner than the designed thickness: around 13.7 µm instead of 20 µm. Figure 9 shows images of cells manufactured with this technique. Note that only 25 to 30 µm of material of the original wafer was consumed in the creation of the cells, leaving 670 µm of silicon for subsequent processing. Further optimization of the KOH release etch should be possible to reduce the amount of silicon consumed in the release process.

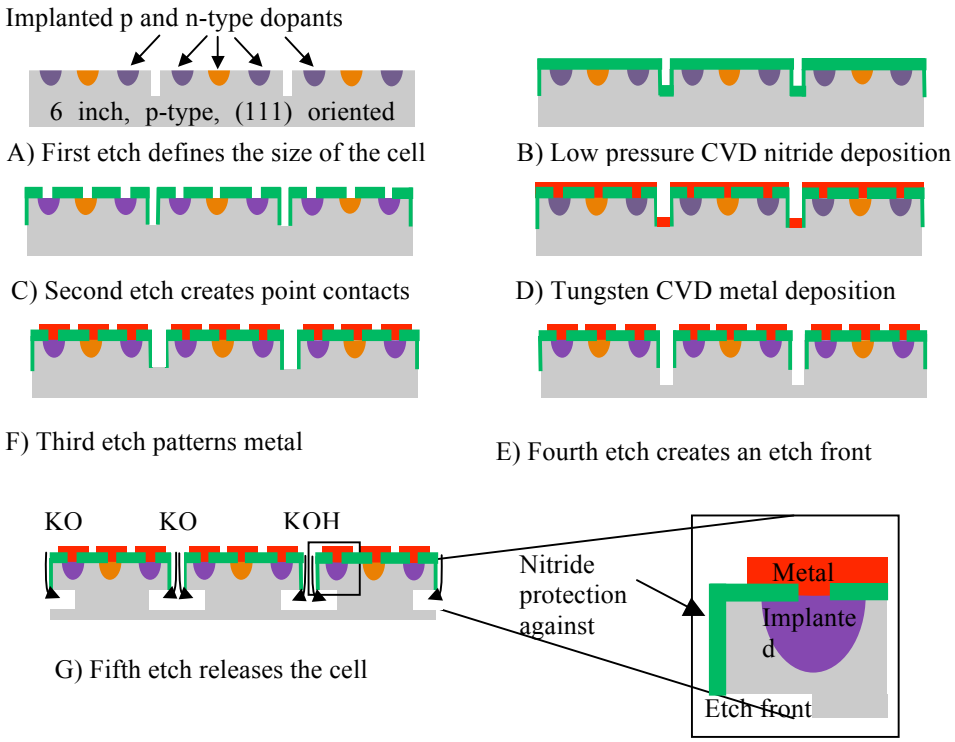
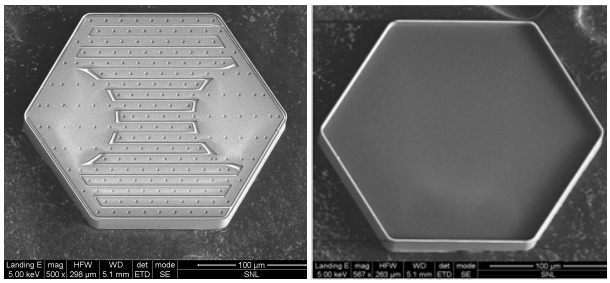


Figure 8. Cross section illustration of the process flow for the creation and release of the cells using a (111) oriented wafer.



(A) (B)

Figure 9. SEM images of the back (A) and front (B) of 250 micron linear contact cells.

4. GALLIUM ARSENIDE CELLS

The single junction, crystalline GaAs cells are created by the traditional approach of epitaxial growth followed by processing to create the metallized contacts. This approach creates a horizontal junction which normally enforces the need for a front and back metal contact, with the front metal contact leading to optical loss. By making the cells very small, it is possible to use a backside contact method that moves all of the metal outside of the optical aperture. (This assumes that the cells are used with some level of concentration.) In addition to avoiding optical losses, the backside contacts will facilitate the packaging of the cells into a module since only one side needs to be interconnected. To our knowledge these are the first fully backside contacted GaAs solar cells demonstrated.

The initial epitaxial layers are given in Figure 10. It should be noted that the cell is designed to be an inverted cell, which allows the backside of the cell to be available for the microprocessing required to create the backside contacts. The

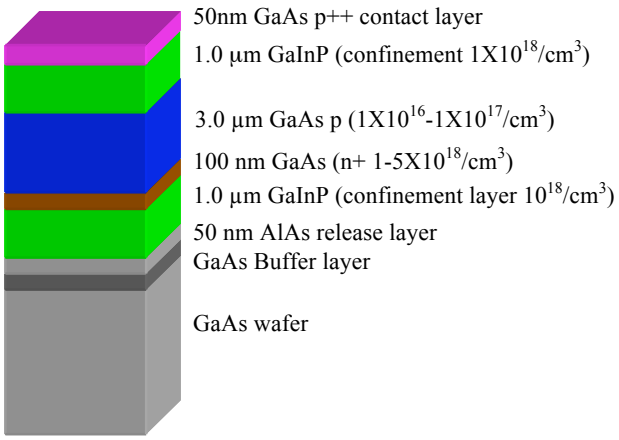
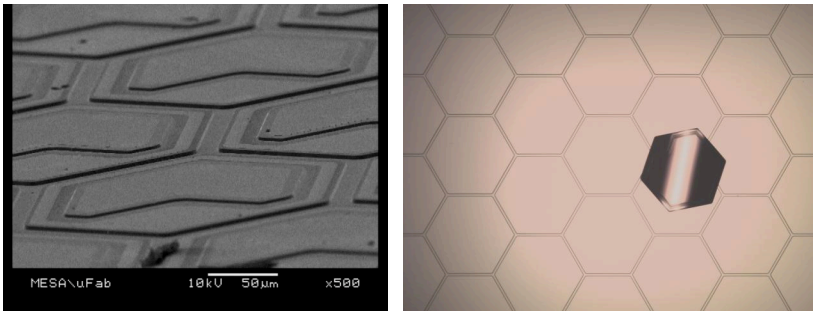


Figure 10. Epitaxial layer stack for the inverted GaAs single junction cell provided by NREL.

epitaxy to create the layers comprising the cell was performed at the National Renewable Energy Laboratory. The microprocessing and cell release were performed at Sandia National Laboratories. The release of the cells is accomplished by including an aluminum arsenide (AlAs) sacrificial layer in the epitaxial stack. The AlAs was selectively etched using a solution of 49% HF in water with Tergitol added to reduce the surface adhesion effects that can cause cells to stick to the wafer after release. Due to the small size of the cells, the lift-off process can be completed in 8 minutes (in contrast to the approximately day long release times required for full wafer epitaxial lift-off[1]). As with the crystalline silicon processes, the remaining handle wafer can be reprocessed to grow and release subsequent batches of cells. Further details of the design and fabrication of the GaAs single junction cells are reported in Cruz-Campa, et al[3].

Recent developments in the GaAs cells include a new residual strain-balanced cell design to reduce the curvature of the cells after release. Also, we have developed a method to achieve much higher doping levels in the InGaP window layer used for one of the contacts, leading to reduced contact resistance between the metallization and the InGaP layer. The reduced contact resistance has improved the performance of the cells. Finally, we have increased the thickness of the absorbing layer of the GaAs cell for further performance improvements. Figure 11 provides some representative images of single junction GaAs cells.



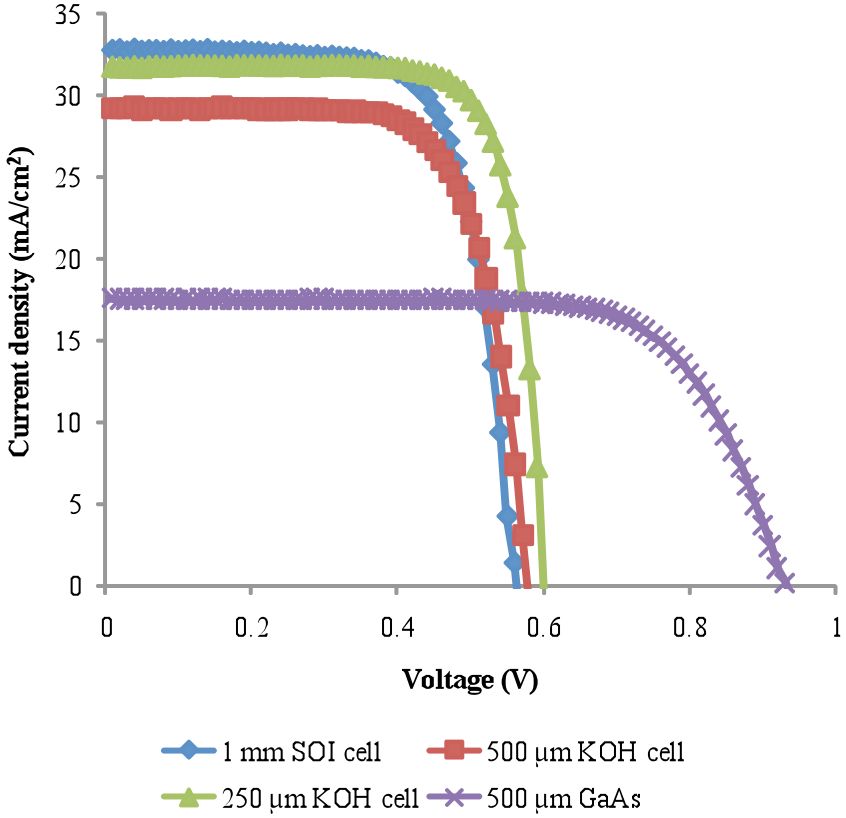
(A) (B)

Figure 11. A) is a SEM image of 250 micron single junction gallium arsenide cells just prior to release. (B) is a 500 micron single junction GaAs cell just after release lying on the remaining substrate (note the slight curvature evident in the cell).

5. SOLAR CELL RESULTS

Prior to testing, the bare release surfaces of the silicon solar cells were treated with a silicon nitride passivating film. The deposition and annealing conditions of the film were optimized empirically to provide good electrical performance. The film thickness was targeted at between 64 and 74 nm to allow the film to also behave as an anti-reflecting coating. After the silicon nitride was deposited, the cells were annealed at 450 °C in a forming gas atmosphere for three hours.

The two different crystalline silicon cells, as well as the crystalline GaAs cells, were then packaged and interconnected for performance testing. JV curves were obtained under ASTM one sun illuminating conditions. We used a Spectrolab model XT-10 with a 1 kW, short arc, xenon lamp, class A solar simulator normalized to 1000 W/m^2 using a silicon reference cell. The beam is an 8" x 8" square, and the chuck is temperature controlled using thermoelectrics. The solar cell was connected through Kelvin probes to a Keithley. Figure 12 depicts the J-V curves of the best performing solar cells to date of both GaAs and silicon.



	250 µm KOH	500 µm KOH	1 mm SOI	500 µm GaAs
Efficiency (%)	14.86	12.03	12.87	11.36
V_{oc} (mV)	597	575	562	930
J_{sc} (mA/cm^2)	31.75	29.29	32.07	17.2
FF (%)	78.4	71.2	71.4	71%

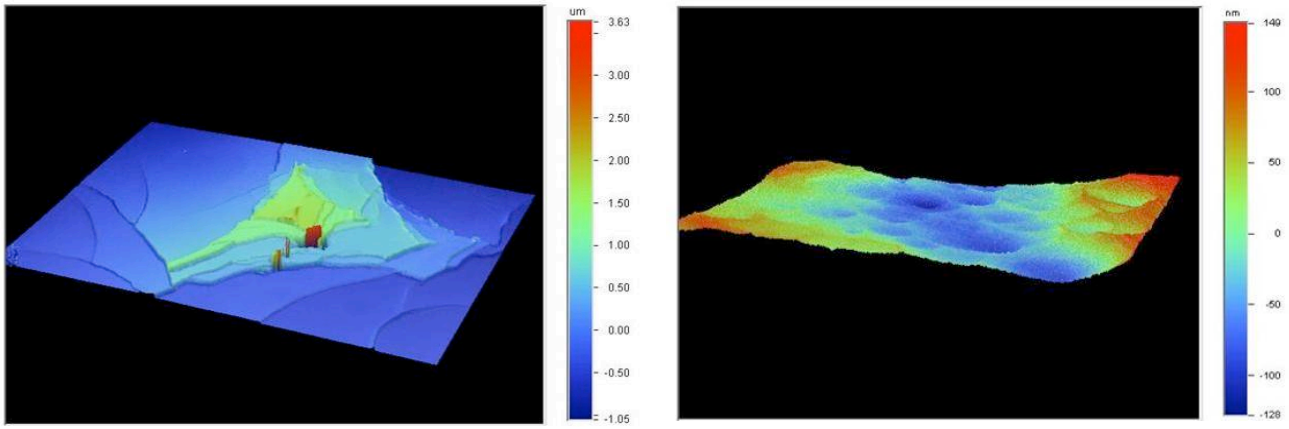
Figure 12. Best solar cell results for different materials and release approaches.

As expected, the GaAs cell has a much higher V_{oc} and a much lower J_{sc} as compared to the silicon cells. This is a direct result of the higher bandgap of the GaAs cell. The total efficiency of the GaAs cell is low compared to other single junction GaAs cells reported on in the literature. Efficiency in excess of 20% would be expected for an optimized cell. The reduced efficiency is a result of a number of effects, including; 1) the cells were tested without an anti-reflective coating on the cells, causing perhaps as much as a 30% loss of light due to reflection, 2) the cell structure includes a 1 µm thick InGaP window layer that absorbs a significant amount of higher energy light before it is able to reach the junction, leading to a significant amount of loss, and 3) even with the reduced contact resistance of the new cells, there still appears to be losses due to series resistance within the cell.

Of the silicon cells, the KOH released cells with the linear contact designs had better performance than the HF released SOI cells. The difference in performance is most likely not due to release technology—we anticipate that either approach

can produce even higher efficiency cells than what we have demonstrated here. There have been some challenges with the metal contacts to the silicon for the HF released cells due to the incompatibility of components of the metallization stack with the HF. This is likely the cause of the reduced V_{oc} and fill factor leading to reduced efficiency of the SOI/radial cells. The Jsc of the radial cells exceed that of the KOH linear electrode cells. This is likely due to the difference in thickness of the two cells. The KOH cells had a thickness of just under 14 mm while the SOI cells were 20 mm thick. The additional thickness improves the absorption of the light, leading to the improved current. In both cells, we observed very good carrier collection which is a result of having the carrier collection locations very close to the point of carrier generation.

The performance of the KOH cells, achieving nearly 15% efficiency, is very good for a silicon cell that is 14 μm thick. The performance is comparable to the majority of commercially produced silicon cells for solar power—yet is more than a factor of ten thinner than those cells. One interesting feature of the KOH cell is that the front of the cell has an intrinsic texture created by the anisotropic nature of the KOH etch. It is well known that texturing the surface of silicon cells enhances the generation of the cell by changing the angle of the incoming light, making it bounce inside the cell, and making it appear thicker. The texture of the KOH cells is noticeable on the front of the cell as displayed in Figure 13. Figure 13 is a 3D optical profilometry image of the topography of the front surface of a KOH released solar cell. Two different types of texture are visible, one at the micron level and another at the submicron level.



(A) (B)

Figure 13. Optical profilometer images from two types of textures observed in the front of KOH released solar cells. A) shows texture at the micron level. B) shows texture at the submicron level.

As mentioned previously, the KOH/linear contact cells had a reduced thickness due to a reduced crystal plane selectivity of the KOH etch. In order to calculate the thickness of the cells created by this procedure, a total of 17 cells were measured with the optical profilometer. Figure 14 shows a 3D optical profilometry picture of the front of the cell, revealing that the thickness of the absorbing material was less than that of the silicon nitride film protecting the edge of the cell. The silicon nitride survived the KOH etch, resulting in the silicon nitride protruding up beyond the height of the resulting cell. On average, the measured thickness was 13.68 μm with a standard deviation of 0.379 μm. The span of thicknesses for all 17 cells ranged from 12.91 μm to 14.3 μm.

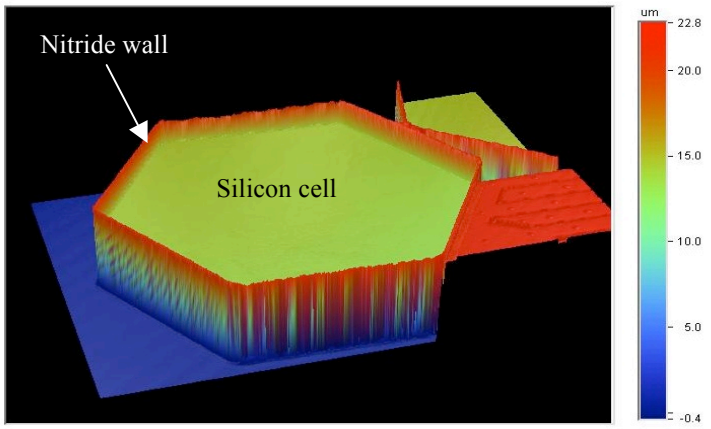


Figure 14. Optical profilometer image of the front of a KOH-released cell.

6. CONCLUSIONS AND FUTURE WORK

We have presented details of the design and fabrication of two different types of crystalline silicon cells as well as a single junction crystalline gallium arsenide cell. These cells have very small dimensions ranging from 5 to 20 microns thick and having lateral dimensions down to 250 microns. The small dimensions of these cells are designed to take advantage of scaling benefits that allow reduced costs, better performance, and new functionality. We have demonstrated solar conversion efficiencies of up to 14.9% with a crystalline silicon cell that was 14 microns thick.

There is significant future work to be done. Additional optimization of the cells to achieve even higher efficiencies needs to be done. It is anticipated that both the silicon cells (with improved light trapping) and the GaAs cells (with the improvements mentioned in Section 5) will be able to achieve efficiencies in the range of 20 to 25%, perhaps higher with optical concentration. In addition to the optimization of the cells, significant work needs to be done in the creation of PV modules based on these cells. The assembly of the cells into modules needs to be approached with consideration of both taking advantage of the scaling benefits of the cells as well as keeping the assembly costs very low. If this can be achieved, the scaling benefits present in PV cells should provide a route to improved PV system performance and, most importantly, significantly reduced costs for solar power.

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